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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,914	08/12/2004	Laura R. Darden	BUR920040177US1	4913

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HOFFMAN, WARNICK & D'ALESSANDRO LLC
75 STATE ST
14TH FLOOR
ALBANY, NY 12207

EXAMINER	
LEVIN, NAUM B	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/710,914	DARDEN ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/710,914 filed on 08/12/2004. Claims 1-20 are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by de Gyvez et al. ("IC defect sensitivity for footprint-type spot defects", 1992).

3. As to claims 1, 8 and 15 de Gyvez discloses:

(1) A method of designing an integrated circuit (IC) design, the method comprising the steps of:

determining net shapes for a net (Often enough, defects reproduce the silicon layer structure of a hard structure yet cause a deviation of the shape of such structure ... A ***fault model*** maps the set of altered hard structures, Rdef, onto the fault class ***F*** – page 641; The first task in this stage is to parse the technology file ... Next, the layout is read and each rectangle is decomposed into horizontal line segments - page 649) (pages 641, 642, 649);

sorting edges of the net shapes in preparation for a plane sweep into a sorted list (the set of horizontal segments sorted lexicographically by ***y*** and **x** coordinates - page 649);

using a plane sweep algorithm to detect an intersection of at least two shapes (The algorithm sweeps each set of susceptible sites by retrieving one susceptible site at a time .... If the new shrunk coordinates intersect each other... page 651) (pages 649 - 652);

creating a new shape from the intersecting shapes in the case that the intersection is not totally contained by one of the intersecting shapes (then the abscissas are expanded by half of the defect size plus the failure criterion. HORIZONTAL) The same actions as with vertical sites, except that the shrinkage takes place on the abscissas and the expansion on the ordinates – page 651), and adding the new shape to an active list of the plane sweep (Protrusion and intrusion defects generated during process step *ti* affect active patterns at the same layer where they occur, and may also have an impact on active patterns at different layers processed at some ***tj, j # i.*** Isolated spot defects do not affect active patterns in the layer where they originated but may affect active patterns in different layers - pages 641-642; we use a linked list of meaningful elements – page 652) (pages 641-642, 651-652);

adding the new shape to a shapes list for the net in the case that the new shape requires a larger spacing than the intersecting shapes (If both ordinates and abscissa intersect each other a valid critical region is formed. Each established critical region is stored - page 651) (pages 651-652); and

routing the IC design and including the new shape on a shapes list for the net as a blockage to prevent spacing errors during routing (the area stage computes the total critical area per defect mechanism, and computes also the partial critical area per

intersection of critical regions with different fault types ... The former area can be used for yield prediction - page 648 ... a series of benchmarks' were implemented in a standard cells place and route approach page 653) (pages 648, 653);

(8) A system of designing an integrated circuit (IC) design, the system comprising (Abstract):

means for determining net shapes for a net (Often enough, defects reproduce the silicon layer structure of a hard structure yet cause a deviation of the shape of such structure ... A ***fault model*** maps the set of altered hard structures, Rdef, onto the fault class ***F*** –page 641; The first task in this stage is to parse the technology file ... Next, the layout is read and each rectangle is decomposed into horizontal line segments - page 649) (pages 641, 642, 649);

means for sorting edges of the net shapes in preparation for a plane sweep into a sorted list (the set of horizontal segments sorted lexicographically by ***y*** and **x** coordinates - page 649);

means for using a plane sweep algorithm to detect an intersection of at least two shapes (The algorithm sweeps each set of susceptible sites by retrieving one susceptible site at a time .... If the new shrunk coordinates intersect each other... page 651) (pages 649 - 652);

means for creating a new shape from the intersecting shapes in the case that the intersection is not totally contained by one of the intersecting shapes (then the abscissas are expanded by half of the defect size plus the failure criterion. HORIZONTAL) The same actions as with vertical sites, except that the shrinkage takes

place on the abscissas and the expansion on the ordinates – page 651), and adding the new shape to an active list of the plane sweep (Protrusion and intrusion defects generated during process step *ti* affect active patterns at the same layer where they occur, and may also have an impact on active patterns at different layers processed at some ***tj, j # i.*** Isolated spot defects do not affect active patterns in the layer where they originated but may affect active patterns in different layers - pages 641-642; we use a linked list of meaningful elements – page 652) (pages 641-642, 651-652);

means for adding the new shape to a shapes list for the net in the case that the new shape requires a larger spacing than the intersecting shapes (If both ordinates and abscissa intersect each other a valid critical region is formed. Each established critical region is stored - page 651) (pages 651-652); and

means for routing the IC design and including the new shape on a shapes list for the net as a blockage to prevent spacing errors during routing (the area stage computes the total critical area per defect mechanism, and computes also the partial critical area per intersection of critical regions with different fault types ... The former area can be used for yield prediction - page 648 ... a series of benchmarks' were implemented in a standard cells place and route approach page 653) (pages 648, 653);

(15) A computer program product comprising a computer useable medium having computer readable program code embodied therein for designing an integrated circuit (IC) design, the program product comprising (Abstract):

program code configured to determine net shapes for a net (Often enough, defects reproduce the silicon layer structure of a hard structure yet cause a deviation of

the shape of such structure ... A ***fault model*** maps the set of altered hard structures, Rdef, onto the fault class ***F*** –page 641; The first task in this stage is to parse the technology file ... Next, the layout is read and each rectangle is decomposed into horizontal line segments - page 649) (pages 641, 642, 649);

program code configured to sorting edges of the net shapes in preparation for a plane sweep into a sorted list (the set of horizontal segments sorted lexicographically by ***y*** and **x** coordinates - page 649);

program code configured to using a plane sweep algorithm to detect an intersection of at least two shapes (The algorithm sweeps each set of susceptible sites by retrieving one susceptible site at a time .... If the new shrunk coordinates intersect each other... page 651) (pages 649 - 652);

program code configured to creating a new shape from the intersecting shapes in the case that the intersection is not totally contained by one of the intersecting shapes (then the abscissas are expanded by half of the defect size plus the failure criterion. HORIZONTAL) The same actions as with vertical sites, except that the shrinkage takes place on the abscissas and the expansion on the ordinates – page 651), and adding the new shape to an active list of the plane sweep (Protrusion and intrusion defects generated during process step *ti* affect active patterns at the same layer where they occur, and may also have an impact on active patterns at different layers processed at some ***tj, j # i.*** Isolated spot defects do not affect active patterns in the layer where they originated but may affect active patterns in different layers - pages 641-642; we use a linked list of meaningful elements – page 652) (pages 641-642, 651-652);

program code configured to adding the new shape to a shapes list for the net in the case that the new shape requires a larger spacing than the intersecting shapes (If both ordinates and abscissa intersect each other a valid critical region is formed. Each established critical region is stored - page 651) (pages 651-652); and

program code configured to routing the IC design and including the new shape on a shapes list for the net as a blockage to prevent spacing errors during routing (the area stage computes the total critical area per defect mechanism, and computes also the partial critical area per intersection of critical regions with different fault types ... The former area can be used for yield prediction - page 648 ... a series of benchmarks' were implemented in a standard cells place and route approach page 653) (pages 648, 653).

4. As to claims 2-7, 9-14 and 16-20 de Gyvez recites:

(2), (3), (9), (10), (16), (17) The method/system/program further comprising the step of checking the design for design rule violations (pages 641-642, 651-652, 655);

(4), (11), (18) The method/system/program further comprising the step of removing the new shape (pages 648, 653);

(5), (12), (19) The method/system/program, wherein the creating step includes assigning edges of the new shape to be distal edges of the intersecting shapes (pages 641-642, 649 - 652);

(6), (13), (20) The method/system/program, wherein the creating step further includes adding a high edge of the new shape (pages 648 – 649);

(13), (20) The method/system, wherein the using, creating and adding steps are repeated (pages 652-653).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N L

Thuando 12/27/06

THUAN V. DO
PRIMARY PATENT EXAMINER